Voltages Before and After Current in HBM Testers and Real HBM

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Abstract - Voltage is a static parameter in present ESD testers and standards with only current specified in time (dI/dt) parameters. Measurements of real and tester HBM discharges identify the previously unknown voltage rate of change (dV/dt) and how this new threat parameter can affect failure levels in some protection circuits.

I. Introduction

Varying ESD failure levels in different HBM testers as well as inconsistency with the TLP tests are becoming more common as ESD protection evolves into increasingly complex circuits, and advanced technologies and lower operating voltages require lower voltages during an ESD event. Because the HBM test is intended to simulate the real HBM event and TLP is intended to provide a similiar threat and to gain insight into HBM, the best reference to resolve all differences is complete knowledge of real HBM event parameters as well as the HBM simulator characteristics and TLP properties. The only ESD rate of change specification since testing began has been applied to the current pulse. The only voltage specification in the test is the DC charge voltage, all other parameters define details of current flow. New measurements of the real "voltage" can now be added to recent measurements of the real current waveform. [1, 2, 3] The complete specifications of the real threat can now be used. The voltage at low levels actually controls the turn on of dV/dt sensitive devices. If these parameters are used to improve the HBM test specifications, ESD designers will have the missing voltage parameters needed for accurate modeling and simulations to develop improved protection circuits.

II. Pre-Post Voltage in HBM Testers.

Early measurements identified HBM tester current waveforms for testing but low level voltages in HBM testers has only recently been reported. Ashton [4], Duvvury [5] and others have measured the initial voltage rise across devices in commercial HBM testers before the well known current pulse and also identified the voltage following the current pulse. One of the more subtle features discovered in the tester was a slowly rising voltage before the HBM current pulse.

A. HBM Tester Measurement Setup

Voltage measurements were made on a 9.4V Zener diode. The diode simulated the turn on of a protection device and also protected the oscilloscope input. Voltages were measured using a 10X passive voltage probe with an impedance of 10MΩ on a Thermo Mk2 HBM simulator. A 4 GHz oscilloscope was triggered using a Tektronix CT1 current probe on one channel of the oscilloscope and the voltage probe was connected to the second oscilloscope channel.

B. HBM Tester Voltage Measurements

Slowly rising voltages across a 10V Zener diode are shown in Figure 1. Any voltage across the DUT is clamped below 10 volts by the zener diode.

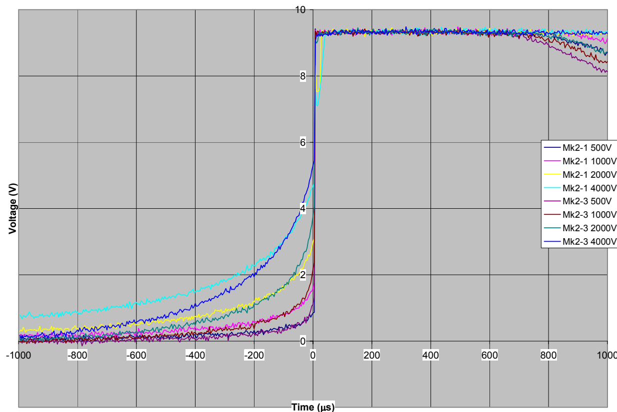

Figure 1. HBM Tester Voltage 200µs per division

The HBM current pulse occurs at t=0 in Figure 1. At the time scale of an HBM event, 100s of ns, the voltage before the HBM current pulse exists for much longer than has been expected in modern circuit design. The pre voltage scales with the HBM charging voltage in the time range of 100 to 1000 µs before the current pulse. For 4000V charging the voltage reaches above 4 volts by the time of the current pulse. When the current pulse occurs at t=0 the voltage is clamped at the Zener voltage for close to 1ms and then decays toward zero over the next 4 ms. The two slightly different exponentially rising waveforms were from two different Mk2 testers manufactured years apart.

The HBM tester has significant board capacitance and the zener diode had about 30 to 50 pF of capacitance. The board and zener capacitance has to be charged by the early initial current.

Adding a resistor in parallel to the Zener diode drains some of the charging current away and reduces the rate of pre current pulse voltage rise. At 10kΩ in parallel with the diode the voltage is almost undetectable.

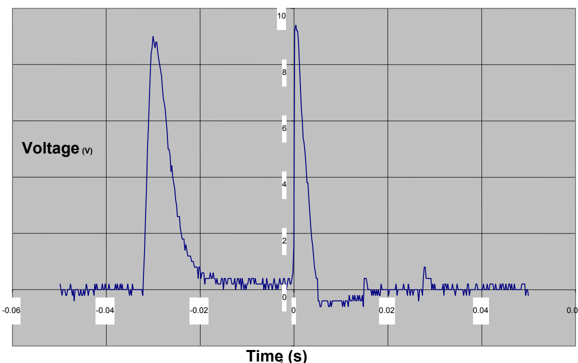

Figure 2. 20 ms /div sweep

Figure 2 above shows an unusual 8 millisecond wide 10 volt impulse 30 milliseconds before the current pulse when producing a test pulse at 1 kV. Some long term measurements of HBM tester voltages show additional short pulses of voltage rising from zero to the 10 volt zener maximum as artifacts. Many details on the voltage rise before and the voltage after the current pulse in HBM testers were reported in the references published in 2004. [4] [5]

III. Pre-Post Voltage in Real HBM

Previous measurements discovered that the current parameters in the real event are controlled by the extremely variable resistance of the ESD spark. [1][2][3] The present specifications for the HBM test were simplistically chosen to be a constant value of 1500 ohms many years ago. Although the resistance at the time of the peak current was a good approximation that point, we have found that before and after the peak current, the greatly changing spark resistance begins with an extremely high resistance. How that resistance changes throughout the discharge determines both the voltage and current waveforms. The change of spark resistance throughout the discharge and the voltage remaining on the charged element (human) obviously determines the time parameters for both voltage and current waveforms.

When the spark resistance begins and ends at extremely high values, the current into the DUT increase and decreases over extremely long periods of time compared to the current pulse. The real HBM voltage begins milliseconds before and ends milliseconds after the pulse current event. The current pulse which causes damage from energy dissipation is specified in nanosecond. Small amounts of current cause no damage from energy; but the voltage they create in an open circuit can affect device turn on, or Time Dependent Dielectric Breakdown (TDDB) of modern gate oxides. [5]. Both voltage parameters are almost 1,000,000 times longer than the existing parameter.

A. Test Configuration

The HBM tester early rise voltage before the current pulse and the voltage following it described above suggested that a measurement of the real HBM threat should be made for comparison. Controlled measurement conditions were assembled with high speed instrumentation to capture all possible data of the real HBM voltage across the zener diode. Figure 3 is a diagram of the real HBM measurement setup and a photo of the measurement setup is shown in Figure 4.

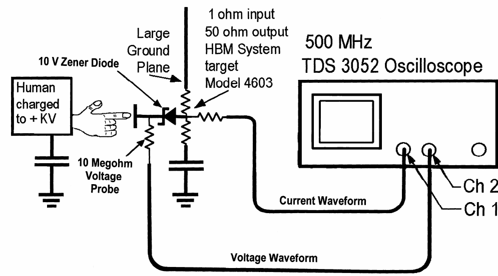

Figure 3. Real HBM V & I measurement circuit

The plastic insulation was removed from a 10 Megohm Tektronix P6139 voltage probe to allow minimum height field disturbances when mounted on the ground plane, shown in figure 4. Conductive adhesive copper foil was placed over the probe projecting through a 2 meter diameter metal ground plane to avoid any current waveform coupling into the high impedance voltage measurement connections.

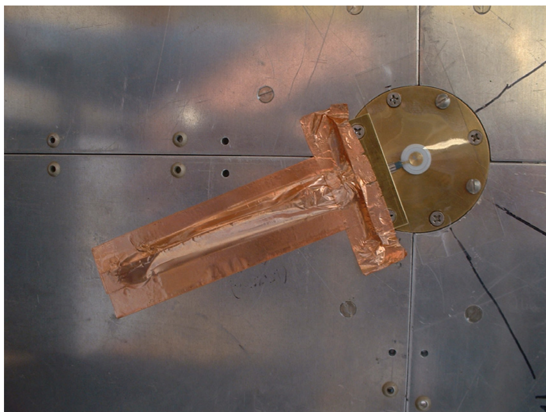

Fig 4. Scope Probe and Zener module on Gnd Plane

A low capacitance (15 pF) sub-miniature 10 Volt zener diode mounted in a Teflon/brass "pill package" was placed in front of a wide bandwidth one ohm current sensor used in earlier measurements of high speed current discharge waveforms. The 10 Megohm probe tip is connected to the zener discharge electrode as shown in figure 4.

A human, insulated from ground by Teflon and Mylar films, was charged for two seconds through a 500 Megohm resistor to specific kilovolt levels, to provide a known ESD level. To create the discharge, the charging voltage was disconnected, and the discharge rapidly made to the brass contact on the zener diode with a finger tip. The current into channel 1 was used to trigger the digitizer sweep, as shown in figure 3.

Measurements were taken during low humidity conditions as were identified in previously reported measurements to achieve the greatest peak current threats. [3] Water dissolved in air inhibits spark formation, and causes the air discharge spark to have a higher resistance throughout its total formation. [6] The actual amount of water in the air, not the relative humidity is important. That value is best identified by the dew point, which is an absolute measure if the total amount of water in grains dissolved in one cubic foot of air. The effect of atmospheric pressure on dew point is minor and will also cause a small effect the spark discharge. Atmospheric pressure differences only have minor effects on the air discharge spark formation. The spark resistance in moist air begins higher, causes much a lower peak currents and extends the current discharge considerably.

B. Real HBM Voltage Measurements

The sweep speed had to be slowed to a few milliseconds per cm. before the extremely slow rate of voltage rise with the 2 ms /cm sweep shown in Figure 5 can be seen. The HBM spark discharge will occasionally drop out as seen in this example about 5 ms after the current discharge. The dropout can occur before or after the current pulse and can be quite variable.

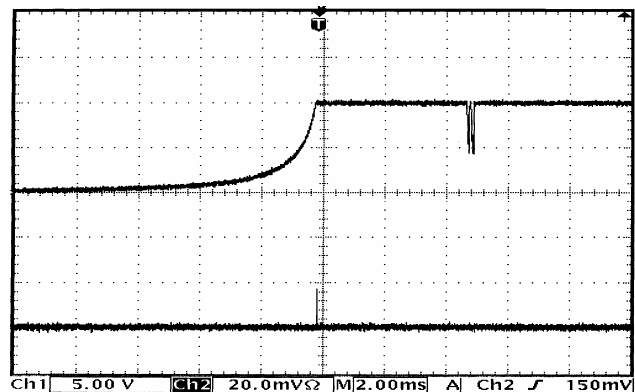

Fig 5. Real Voltage Ch 2 top, Current Ch 1 Bottom

Figure 6 shows the same exponential rise but at 20 ms per cm sweep shows the voltage lasting for over 100 ms. Voltages lasting for 20 to 200 ms after the current pulse appears to depend on the maximum spark resistance.

The voltages across the 10 volt, 15 pF zener diode were loaded with the 10 Megohm shunt resistance of the voltage probe. Without added shunt resistance the voltage across a low leakage zener or snapback device could remain at 10 volts even longer. As mentioned above, spark discharges in air with higher humidity levels begin at much higher resistances and increase

from there. Further measurements with higher resistance voltage probe made at higher humidity levels are needed to identify the maximum time that Vt1 voltages will remain across snapback type protection circuits after the current pulse. Further measurements with less loading of the exponentially rising voltage or device capacitance can also identify the earliest and slowest voltage rise time which will occur before the current pulse.

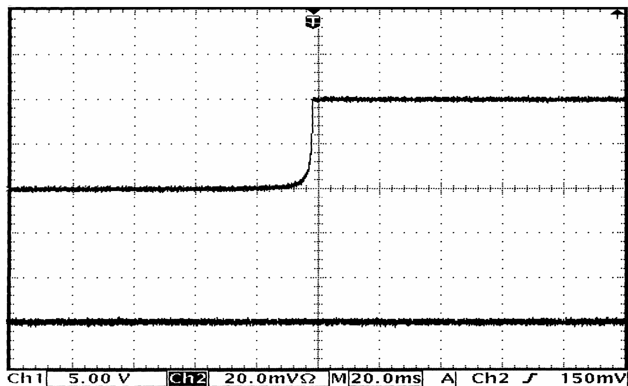

Fig 6. Real Voltage Ch 2 top, Current CH 1 Bottom

Milliseconds before the current pulse occurs, extremely low current flowing into the low capacitance of a high impedance, non-conducting, protection circuit, or in this measurement, the non-conducting zener diode, cause its voltage to build up extremely slowly. Figures 5 and 6 show the slowly rising voltage typically measured across the zener diode used to simulate an ESD protection circuit. Protection circuits are non-conducting until current begins to be drawn at slightly below the point identified as Vt1 in TLP analysis.

The real HBM spark resistance after its minimum shows abrupt changes which make the recordings appear rather "noisy". The measured abrupt current increases and decreases occur in a random manner, although the general trend of current decays is followed to completion. Occasionally short impulses of current are seen in the 0.1 to 2 millisecond range after the current appears to have terminated. This could be resistance from direct finger contact being made some milliseconds after the charge voltage has decreased to the point where sparks can no longer form.

The real HBM voltage impulses are quite variable from pulse to pulse but can be rather similar to those found in HBM testers. The HBM tester artifacts or random voltage pulses are repeatable for each pulse; however the real HBM event can have great random voltage pulse variations from pulse to pulse some milliseconds after the current pulse.

That investigation identified the rate of voltage rise in real HBM discharges as being extremely slow. The upper plot in Figures 5 and 6 are the voltage waveforms measured on channel 2. They are typical of many 1kV discharges, although at this charge amplitude the voltage across the zener diode sometimes only rises part way to the 10 volt level of the zener diode, before a fast current pulse occurs.

At 2 or 3 kV human body charge amplitude the voltage rises sooner and is clamped at the 10 volt level many microseconds before the much faster current discharge rise of the pulse occurs. Higher charge voltages create earlier exponential rising voltages which reach the clamp voltage limit before the current pulse begins. The bottom trace of figure 5 is of the current pulse on channel 1. This event can be missed because of the extremely slow sweep speed needed to record the complete voltage rise. An additional digitizer was used in these testes to verify that each measured pre and post voltage, had the typical peak current and decay observed of real HBM discharges. The current waveform was split and triggered both digitizers identically, but the current waveform verification digitizer used a much faster, 4 ns /cm sweep.

IV. ESD Discharge Phase Analysis

Our analysis of the measurements of the voltage and current from real HBM events can be described as having three different phases from three different electrical effects. The cause of the slow positive exponential voltage rise first phase needed to be identified. To eliminate the part of the rising voltage caused by avalanche current from an air spark discharge, measurements of the early voltage rise of a test pulse produced by a vacuum relay were made.

A. Phase 1, dC/dt, Displacement Current Causes Increasing Voltage into an Open Circuit

The voltage which rises long before the current in a closing mechanical switch was shown to be caused by a displacement current in the vacuum relay experiment. A displacement current is created across the switch contacts as they approach each other and the capacitance between them increases. One contact moving toward the other produces a current flow into the open circuit DUT, creating a voltage which increases until a voltage limit is reached and shunt current to ground limits further voltage increase.

1.Vacuum switch measurement Setup

A high vacuum relay was used, to isolate ionization effects in a gas as contacts move toward each other. It simulated the first phase of a charged finger moving toward an open circuit pin of an IC. Vacuum relays have extremely high voltage standoff capabilities because there is no gas between the electrodes to ionize. Figure 7 below is a diagram of the circuit using a vacuum relay to examine the positive exponential voltage rise similar to that found in real HBM discharges and HBM simulators. Any current flow from increasing capacitance between closing contacts in a vacuum relay must be caused by a displacement current. When the relay contacts physically touch a current pulse into the one ohm current sensing resistor provided a trigger voltage. The 10 Megohm probe recorded the rising voltage across the 15 pF zener diode limited to 10 volts until the current pulse occurred.

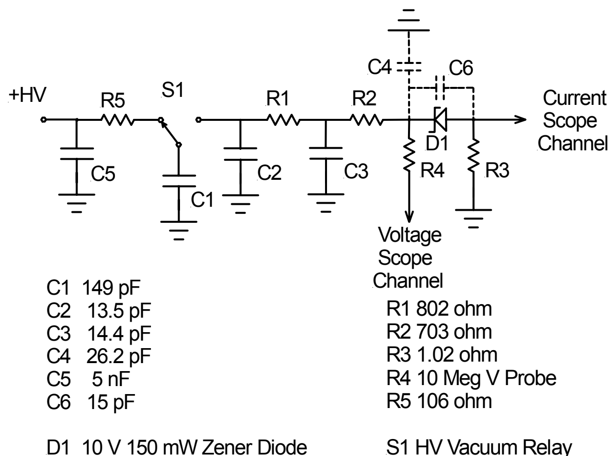

Figure 7. Vacuum Relay discharge circuit

2. Data from vacuum switch Early Voltage Rise from dC/dt

Figure 8 shows the digitizer recordings from the circuit in Figure 7. The top waveform on channel 2 measured a positive exponential voltage rise to the 10 volt limit of the zener diode. The bottom trace on channel 1 barely shows the much shorter current discharge at the center of the screen. This 1 kV measurement shows the initial voltage rising to the 10 volt limit of the zener diode about 100 microseconds before the current pulse. The rising voltage is clamped at 10 volts 480 microseconds before the switch contacts close when tested at 3 KV. Figure 8 is one of over 20 measurements made of voltage induced into the low capacitance high resistance load as the contacts move toward each other. The waveforms were so repeatable that many pulses could be averaged to improve the signal to noise ratio of the measured data.

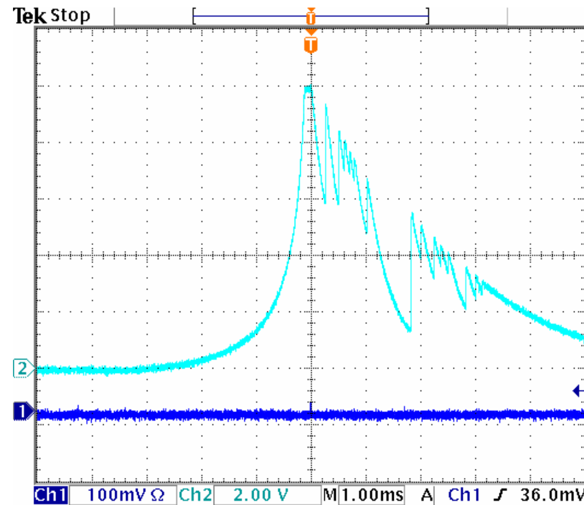

Figure 8. 10 Volt maximum rise from moving charged contact.

These measurements consistently showed the voltage rising exponentially. The current obviously begins at picoamps, and increases slowly sometimes to a fraction of an amp before an abrupt increase in current when the contacts connect. The charge supplied to the Zener by the displacement current before the main current pulse became large enough that it could even be detected by the 1 Ohm current sensing resistor R3, especially when the Zener breakdown voltage was reached.

The voltage trace after the 10 volt level is not important and simply shows the voltage decay during the many vacuum relay contact bounces. In a vacuum relay without a gas to ionize between discharge electrodes, current flow only occurs when metallic contact is made discharging capacitor C1.

When the voltage reaches 10 volts across the 10 Megohm loaded, 15 pF zener diode, the displacement current from the increasing capacitance has already increased to more than one micro amp. These measurements highlight an important fact to consider when analyzing the possible voltage increase on low leakage pins of an IC from real ESD events. Pico/nano amps of current have milliseconds to charge an “unloaded” open circuit low capacitance pin and would cause the voltage to rise significantly earlier than measured here with the 10 Megohm shunt resistance across the open circuit DUT.

Additional measurements are needed to determine at what transition point the current changes from displacement to ionization electron current flow which occurs for real HBM and HBM simulators

using gas filled relays. This experiment clearly shows that switch contacts moving toward each other have a sufficient amount of increasing capacitance to force enough current into the capacitance of the DUT, to cause the voltage to rise to 10 volts long before the rapid avalanche current increase occurs and the peak current is reached.

3. dC/dt Model Analysis

A simple contact dC/dt model was created to see if it could reproduce the initial voltage seen in HBM testers. Fig. 9 shows a circuit diagram of the model in which Vc is the voltage on the HBM capacitor, C_R is relay contact capacitance, R_L is the load resistance across the DUT pins, and C_l is the load capacitance across the DUT pins. The HBM capacitor was treated as a voltage source since very little charge is lost during the pre discharge phase. Also, the voltage drop across the HBM 1.5kΩ resistor is negligible and therefore was neglected in this analysis. For the relay contact capacitance a parallel plate model was used and it also assumed that the relay contact closure velocity was constant.

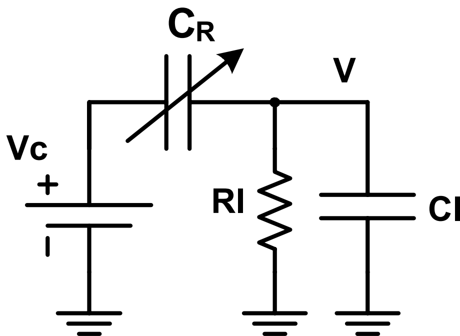

Fig. 9. Schematic diagram of the dC/dt contact closure model

The equation for the current is therefore

$$i = -\frac{\varepsilon_o A}{d_o - vt}\frac{dV}{dt} + (V_c - V)\frac{\varepsilon_o A v}{(d_o - vt)^2} = \frac{V}{R_L} + C_l\frac{dV}{dt} \quad (1)$$

where

ε_o = permittivity of the relay gas,

A = area of the relay contacts,

v = the closure velocity of the contacts,

V_c = the HBM charging voltage,

d_o = the initial relay contact spacing, and

V = the voltage across the DUT pins.

The first term or the dV/dt term of Eq. 1 is weaker than the second term or the dC/dt term and the current into C_l is smaller than the current into R_L even for values on the order of 1MΩ. Thus, Eq. 1 can be simplified to

$$i = (V_c - V)\frac{\varepsilon_o A v}{(d_o - vt)^2} = \frac{V}{R_L} = (V_c - V)\frac{Kv}{x^2} \quad (2)$$

where $\varepsilon_o A = K$ and $d_o\text{-}vt = x$. The solution to Eq. 2 is

$$V = \frac{R_L K v}{x^2 + R_L K v}V_c = \frac{V_c}{1 + \alpha x^2} \quad (3)$$

where $\alpha = 1/R_L Kv$.

Fig. 10 shows data taken from an HBM tester (points) and a fit of the data based on Eq. 3. The parameters used to fit the data include and a contact distance of 100µm at t = -1ms, a final contact distance of 15µm at t = 0, which is the starting point of the main discharge, a contact diameter of 0.3mm, a permittivity of free space, and a relay contact closure velocity of 8.5cm/sec. Note that Eq. 3 fits the data quite well using reasonable fitting parameters. Thus, the dC/dt theory of the initial voltage build up on a DUT pin of an HBM tester appears to be valid.

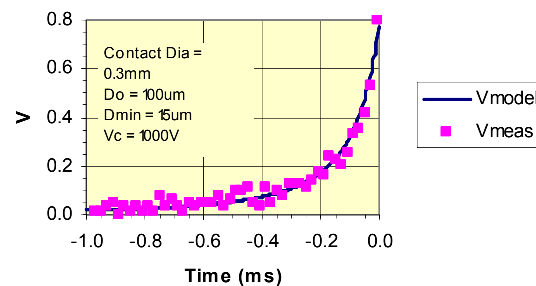

Fig. 10. HBM tester data points and model fit of the initial voltage build up

Data taken using the vacuum relay setup, as described in section 1, was also studied. In theory, the contacts of the vacuum relay don't arc as the contacts approach each other until the contacts are within microns of each other when field emission starts occurring. Fig. 11 shows a plot of the voltage developed across the voltage scope probe versus time for a charging voltage of 1000V. Also shown in the figure is a curve generated from a solution of Eq. 1 using a numerical integration. The load capacitance included the sum of C2, C3, C4, and C6, which is 69pF. R1 and R2 where assumed to be negligible. The load resistance for this case was the oscilloscope probe resistance, which was

10Meg-Ω. The curve fitting parameters include the stopping distance (Dmin) or the distance where the main discharge is initiated and the contact closure velocity. The simulation time, the contact closure velocity, and the final distance were used to establish the initial contact distance, d_o. The measured diameter of the contacts is 1mm. For this simulation a good fit is seen with a contact closure velocity of 1.9cm/sec, a simulation time of 5ms, a d_o of 100μm, and a final distance of 5μm before the main discharge begins.

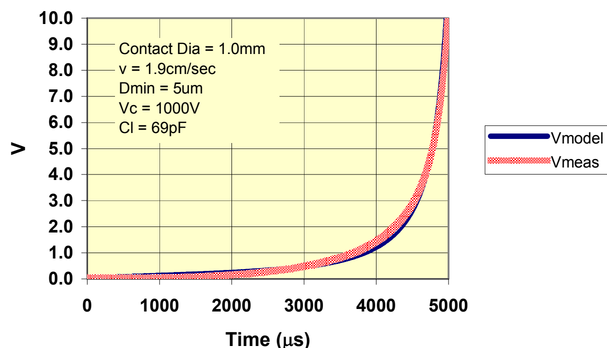

Fig. 11. Measured and calculated pre contact closure voltage curves for a vacuum relay.

Fig. 12 shows a plot of the calculated capacitor and load resistor current vs. time. For this case the load capacitance absorbing more of the current than the load. Note that the dC/dt current of the contacts is on the order of μA.

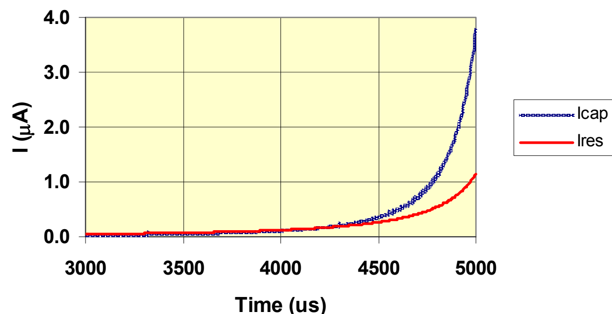

Fig. 12 Calculated current flowing into the load resistor (10Meg-Ω) and load capacitance (69pF).

These measurements and calculations were repeated with an addition of a 1Meg resistor placed in parallel with the scope probe, producing a net load resistance of 0.909Meg-Ω, and with the charging voltage increased to 4000V. For this case the voltage is held to a lower value until the contacts get very close to each other. Also, the resistive current is much higher than the capacitive current and the overall current is higher than the previous case due to the higher charging voltage. The calculated results for this case also closely followed the measured data.

In conclusion, the model, Eq. 1, can be made to closely follow the measured time voltage curve that exists prior to the main discharge of a capacitor using a relay. The fitting parameters, the final contact separation distance before initiation of the main discharge and contact closure velocity parameters used in the curve fitting appear reasonable.

B. Phase 2, Initiation of Ionization Current

The second phase of the ESD event is a very rapid rise of electron current flow between finger and DUT pin through ionized air or ionized gas between switch electrodes as the gap between the charged and uncharged contacts decreases to the self breakdown point. An avalanche discharge electron current begins at extremely low currents of some multiple of electrons. The spark resistance at this point is extremely high but avalanche discharges proceed rapidly to its minimum resistance and maximum current. A gas insulated gap, will ultimately break down when the self breakdown voltage is reached and an avalanche discharge begins.

C. Phase 3, Increasing Spark Resistance

The ESD spark resistance has been earlier shown to increase as the current through it decreases. [3] This effect is clearly seen in figure 13. More sensitive measurements in the milliamp range show very similar non constant exponential rates of decay. This leads to the conclusion that the decreasing current causes the spark resistance to increase to at least 10^8 ohms before the discharge terminates.

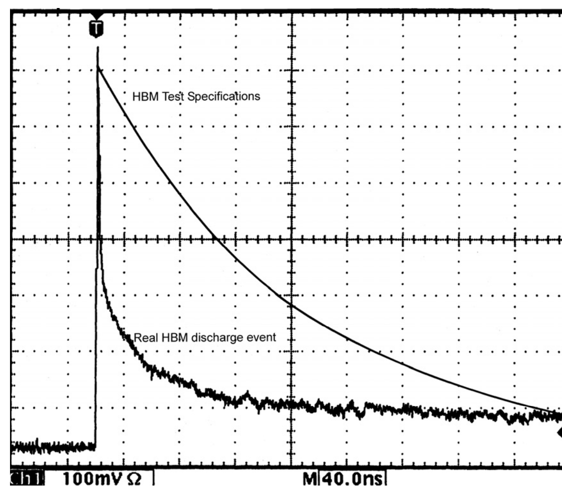

Figure 13. Real HBM/1500 ohm decay rates

Figure 13 shows measured real HBM current decay rate compared to the constant 1500 ohm resistance in the HBM test specifications. It is obvious that the current decays faster and will last longer than that in the HBM test. Simple analysis of the real HBM current decay rates clearly indicates that the resistance of the spark increases throughout its duration. Similar waveforms measured at longer times and lower currents provide very similar non-constant RC decay rates which also appear to continue for as long as the spark discharge continues. These measurements, although difficult to make at very low currents, give good indication that while the resistance of the spark in dry air can be as low as 1000 ohms, it will increase many orders of magnitude until it terminates.

The voltage measured across the zener diode remained at the zener voltage for 10 to as long as 100 milliseconds. Because the voltage was clamped by zener conduction currents there was obviously current flowing into the zener diode. Therefore the charge voltage had to be above 10 volts while it was clamped at the zener voltage.

D. Phase Plots

The length of time that voltage exists across a 10 volt zener diode must be supplied by current flowing into it. The real HBM discharge resistance must maintain at least the 10 volt current clamping level. Preliminary analysis of the spark resistance from measurements milliseconds after the current pulse, puts it at many Megohms. A plot of the resistance when the HBM event begins and when it ends can look like Figure 14 below.

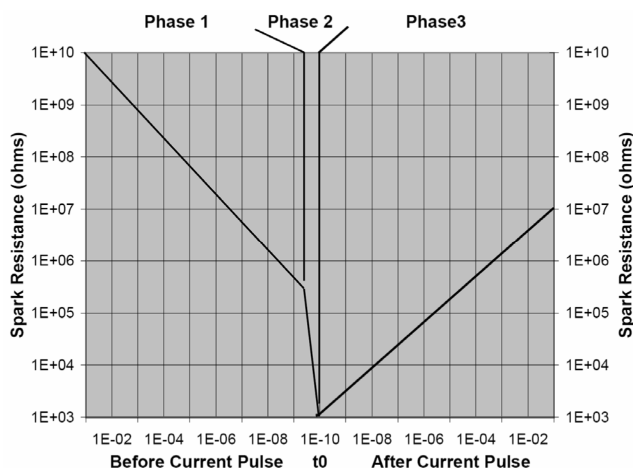

Figure 14. Effective source resistance of the HBM Event

V. Effects of Pre/Post Voltage on ESD Protection and Core Circuits

A. ESD protection circuits sensitive to dV/dt

1. Dynamically Triggered Clamps

There are a number of dynamically triggered clamps whose performance is adversely affected by a slow build up of voltage just prior to the main HBM discharge. Two such clamps that will be examined here are the gate pull NFET snap-back clamp and the transient triggered clamp or BigFET.

Fig. 15 shows a schematic diagram of a gate pull snap-back NFET. It was shown by Duvvury [7] that by applying a small gate voltage, around 1.5V, to the gate of an NFET caused its drain to trigger at or near the snap-back holding voltage rather than at the grounded gate avalanche breakdown voltage. Eliminating the negative resistance region promotes uniform triggering of the fingers and also guarantees that the “snap-back” clamp does not trigger ahead of an I/O driver transistor.

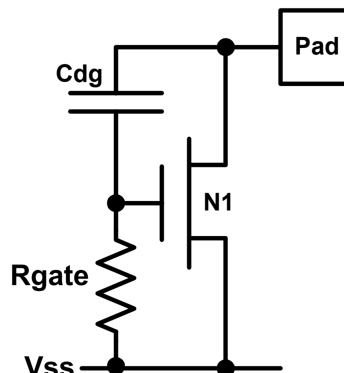

Fig. 15. Schematic diagram of a gate pull NFET pad clamp

The small gate bias is applied dynamically by coupling the drain voltage to the gate via a drain to gate capacitance, Cdg. The objective is to get the gate voltage to around 1.5V when the drain is at or near the snap-back holding voltage. In most cases, especially for 3.3V transistors, the natural drain to gate overlap capacitance provides sufficient drain to gate coupling to make an external capacitor from the drain to the gate unnecessary. A resistor is used to pull the gate of the clamp transistor to ground during normal operation and just before ESD events. Variations on the grounding means for the gate of the NFET clamp include a ground switch transistor enabled by the presence of a Vdd voltage.

It can be seen from Fig. 15 that if there is a slow rising pre-discharge voltage on the drain such that the rise time of the pre-discharge voltage is longer than the $R_{gate}C_{gs}||C_{dg}$ time constant then the gate voltage will be sitting at 0V with an initial voltage just prior to the main discharge appearing on the drain. Thus, the drain voltage swings not from ground but from some initial voltage to the desired trigger voltage. If the desired trigger voltage is, say, 6V and the initial voltage is 2V then the drain voltage swing during the main discharge rise is 4V and not the 6V if the initial voltage were 0V. This reduced swing lowers the gate voltage corresponding to the desired drain trigger voltage.

A Spice simulation was performed on a 3.3V NFET with a channel length of 0.35µm and a channel width of 400µm (N1 of Fig. 15). No external capacitor was used thereby relying on N1's natural gate to drain capacitance. The gate was attached to a 100kΩ resistor to ground. The gate voltage is assumed to be at 0V at the threshold of the main HBM discharge thanks to R_{gate}. The voltage on the drain was raised from some initial value to 6.2V, the target drain trigger voltage. Fig. 16 shows a plot of the gate voltage at a drain voltage of 6.2V versus the initial voltage. The equation describing this curve is

$$V_{gate} = \frac{C_{dg}}{C_{gs}}\left(V_{drain} - V_{initial}\right) \tag{4}$$

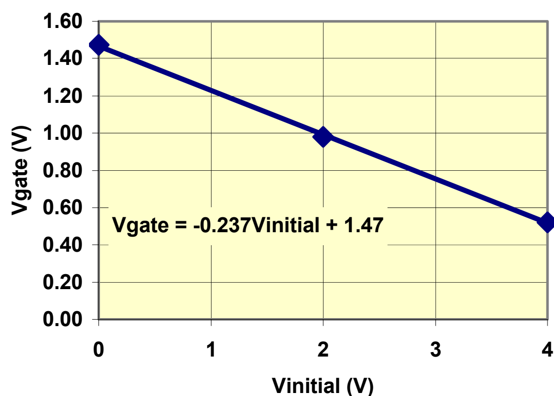

Fig. 16. Plot of gate voltage versus initial drain voltage for a target drain trigger voltage of 6.2V

Thus, the slope of Fig. 16 is given by the ratio of drain to gate capacitance to the gate to source capacitance and the offset term by the product of the capacitance ratio and the drain target voltage. In going from an initial drain voltage of 0V to 2V the gate pull voltage at 6.2V on the drain goes from almost 1.5V to a little less than 1V. Thus, as the initial voltage increases the gate pull up voltage decreases causing an increase in the trigger voltage and an increase the likelihood of conduction non-uniformity in the NFET clamp.

Fig. 17 shows the schematic diagram of a single inverter BigFET or transient power bus clamp. For normal operation during an ESD event, the voltage between Vdd and Vss is assumed to be 0. If the voltage rapidly rises (in a few 10's tens of nanoseconds or less) the voltage on node 3 will be held to Vss via the timing capacitor, M2. Thus, the voltage on node 2 will be at Vdd thereby turning on the "BigFET" transistor, M5, which shunts the ESD current from Vdd to Vss. If the voltage applied to Vdd lasts long enough (1 µs or more) M3 will pull up node 3 to Vdd thereby turning off M5. Thus, the shunting action of M5 lasts for only a short period of time, but long enough to last throughout the discharge of an HBM event.

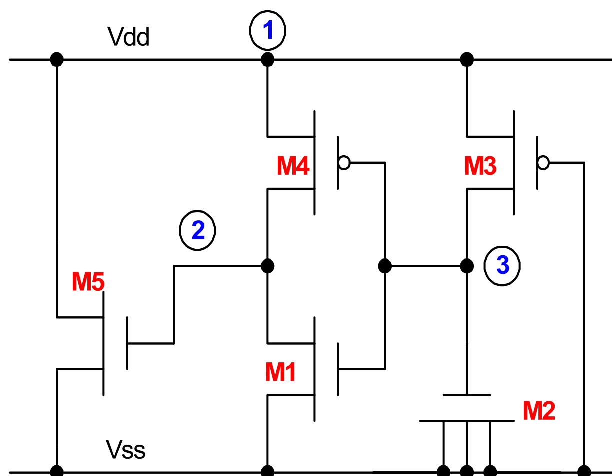

Fig. 17. Schematic diagram of a single inverter BigFET

If a voltage is slowly applied to Vdd such that node 3 tracks with Vdd, then there is no current shunting and M5 remain "off". Thus, a precharge voltage acting over several milliseconds will not be inhibited by BigFET. If there is a voltage appearing on node 3 just prior to the main HBM discharge then this voltage will remain on node 3 during the peak voltage and current of the discharge. Thus, M5 is held off for voltages up to and somewhat beyond the voltage on M2. For M5 to turn "on" the voltage on Vdd must be high enough, generally somewhat higher than the sum of Vt of M4 plus the voltage on the gate of M2, for the inverter comprising M1 and M4 to transition to the 1 state on its output thereby turning M5 "on". This delayed turn on due to a precharge voltage allows a

higher voltage to appear on Vdd during the main HBM discharge, which lowers the protection level.

Fig. 18 shows a BigFET simulation under an HBM discharge with different initial voltages applied and with a current rise time of 10ns. The initial voltages included 0, 1, 2, 3, and 4V. One very apparent observation is that there is a lack of a complete discharge due to the timer turning the BigFET off before the HBM capacitor is thoroughly discharged. For the 4V curve one can see that the voltage rises after the BigFET shuts off due to several volts of remaining charge on the HBM capacitor. Thus, an initial voltage impressed across a BigFET can result in an incomplete HBM capacitor discharge, which leaves a significant, and possibly damaging residual voltage.

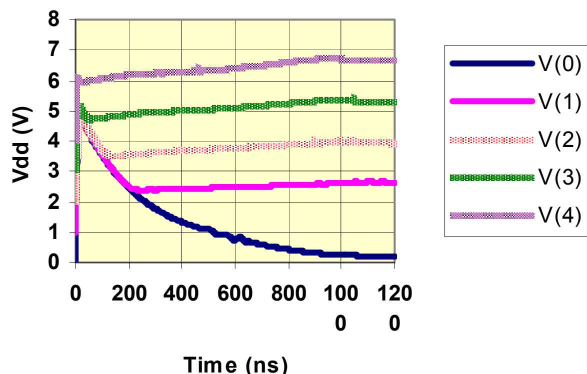

Fig. 18. BigFET response for different values of initial voltage

It was found that a plot of Vdd versus time for a BigFET with 3 inverters instead of 1 inverter between the RC timer M2-M3 of Fig. 17 and the big NFET clamp M5 resulted in a plot similar to Fig. 18 when the initial Vdd voltage was set to 2V. However, when the initial Vdd voltage is increased to 3V oscillations are seen as shown in Fig. 19. Interestingly, the residual voltage is about 0.5V, which is much lower than for the 1 inverter case. However, the oscillations produce spikes of up to 6.35V, which is well above the peak voltage of 5.4V for the 1 inverter case. One of the authors has seen oscillations in 3 inverter BigFETs when trying to do DC leakage measurements. The oscillations are no doubt due to the high source resistance of the HBM in conjunction with the phase shift associated with 3 inverters and the large clamp transistor. A 1 inverter BigFET, however, cannot oscillate under any circumstance.

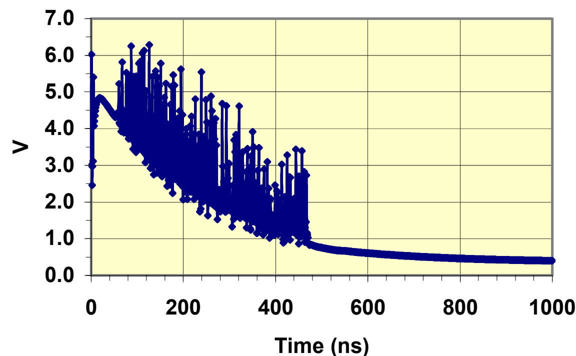

Fig. 19. 3 Inverter BigFET response for an initial voltage of 3V

Although the dynamic circuits shown here have performance degradation due to the slow build up of an initial voltage due to relay dC/dt, the charge associated with this build up can be shunted by a relatively large resistor or leakage current to a point where the initial voltage has a relatively small effect on performance. BigFETs, for example, are placed across power supply terminals, which, in most cases, have enough leakage to keep the voltage build up small. Furthermore, a large shunt discharge resistor such as that described in Merrill[8] can be placed across the power supply terminals with a negligible effect on operating power. The most sensitive case is where a “hot pluggable” input has only a dynamic gate pull NFET for protection with no diode to Vdd. In this case the leakage can be very low which will allow a full build up of voltage on the input node. Solutions include adding an external capacitor between drain and gate to increase the pull up in the advent of a large initial voltage or using a static threshold device between the drain and gate such as a number of series diode connected MOSFETs.

VI. Summary

This paper explores the origins and examines the causes of HBM voltage rise/decay in both ESD simulators and in real HBM. The measurements of real and HBM testers now identifies the dV/dt rate as being extremely slow, in the millisecond range, and occurs long before the presently specified current pulse and remains long after the peak pulse current.

VII. Conclusion

Early IC's were Bipolar, operated at 15 volts and had very large structural features. Modern protection circuits for IC's have evolved into CMOS of deep sub-microns sizes which now operate at three volts and below. ESD designers developing ever improved protection circuits have been working on the incorrect assumption that the voltage across a device rises in sub-nanosecond or ten nanosecond rates.

Voltage data allows ESD designers to be aware of dV/dt parameters of the Real HBM event that are not presently used in the ESD standards for qualification of devices. The present discharge time parameters specify only the current waveform, omitting this extremely slow dV/dt rate of rise which occurs in the real world. Ignorance of the dV/dt parameters have inadvertently resulted in many problems over the years with qualification of product, and will become increasingly important in the years to come as device geometries continue to get smaller. It is has been recently shown that removing the Pre/Post (P2V) portions of the ESD threat in existing testers, will allow devices susceptible to this threat to pass qualification. However, in the long term, it will become important to make sure that testers include these threats in a controlled and reproducible manner to qualify products to threats that simulate the real world.

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